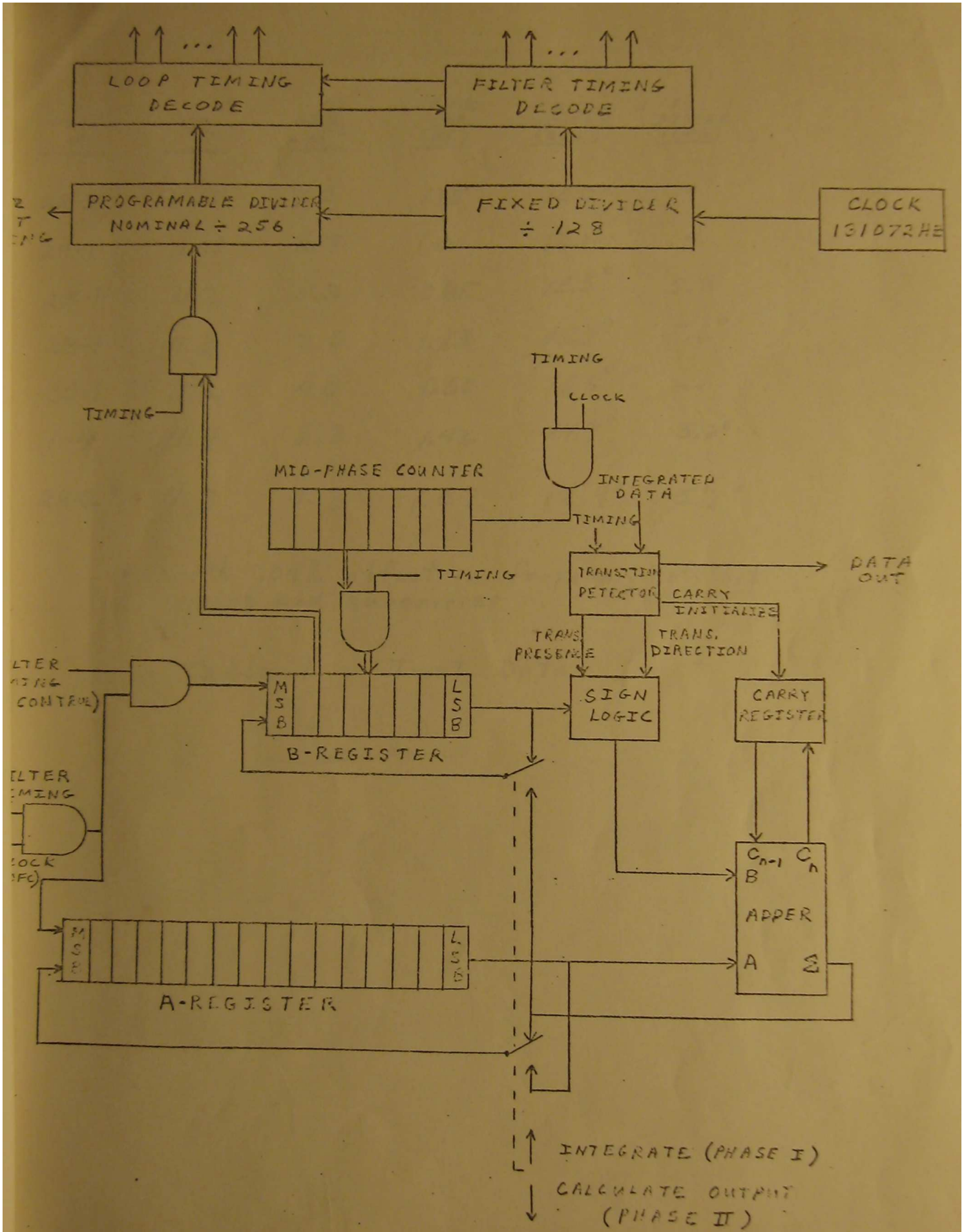
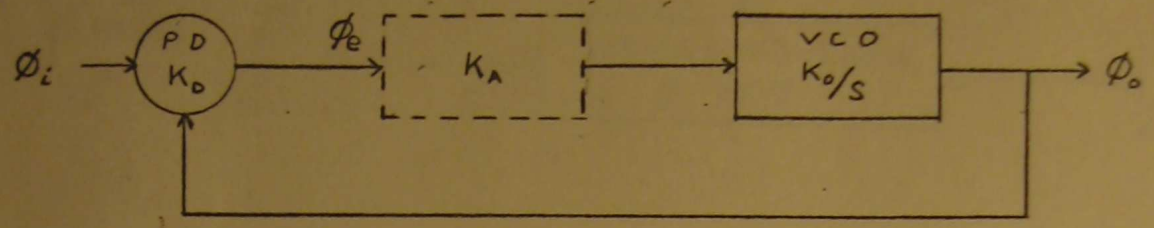


FIGURE 1-C: BLOCK DIAGRAM, BIT SYNCHRONIZER (SECOND ORDER)



$K = K_o K_D K_A$ $\quad H(s) = \frac{K}{s+K}$ $\quad B_L = \frac{K}{4}$ (Hz) single sided

$K_o = 4$ $\quad K_D = 1$ $\quad K_A = 1/4$

Fig 1-A : First Order PLL

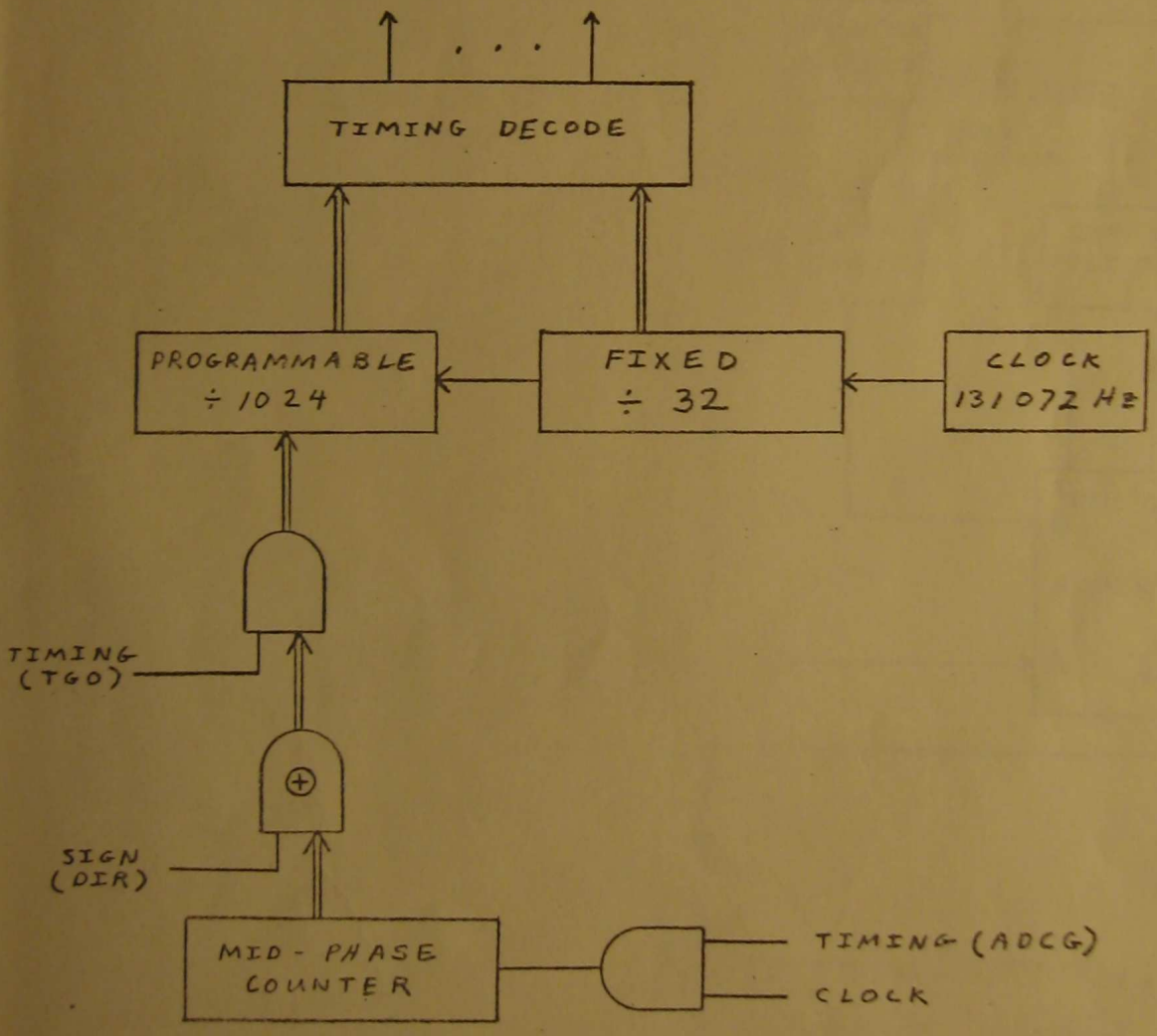


Fig 1-B : Digital Loop

FINAL ENGINEERING REPORT

VIKING LANDER COMMAND DETECTOR BREADBOARD DESIGN EFFORT

Report Prepared By: R. Schuster

Contributors

R. J. Fox
J. Reid

June 10, 1971

Organization of Report

This report describes the circuits and techniques used to implement a Single Channel Command Detector for use in the Viking Lander System. Section 1.0 contains an abbreviated theory of operation for both the Mariner 69 and Viking Command Detectors for comparison purposes.

Section 2.0 goes into more detail with respect to system operation and reviews some of the system parameters.

Section 3.0 is a detailed description of the circuits presently used in the breadboard. Schematics and logic diagrams are presented along with the important system timing diagrams.

Section 4.0 reports on the breadboard test effort and includes a description of the test technique and methods of implementing the tests. Test results are presented and discussed. The results of an analysis of the transient behavior of the Bit Synchronizer Loop (BSL) are presented.

Section 5.0 delineates recommendations for design changes which will improve the performance or reliability of the Command Detector.

Section 6.0 contains the main conclusions of the report.

Wide confidence intervals such as the aforementioned would make detection of changes in error rate impossible to detect when design parameters are to be adjusted for lowest error rate. It was for such reasons and simply because of the economic considerations in running such long tests that an investigation was undertaken to find a better method of testing the Command Detector. This effort is described later in this report.

1.2 Background (Technical)

1.2.1 General

The breadboard design described here is briefly compared with the Mariner 69 Command Detector. This comparison is intended only to show the major differences in approach to the detection problem.

Mariner 69

The Mariner 69 Command Detector derives bit timing from a synchronization signal which is transmitted along with the command data. The timing recovery is therefore independent of data structure and in fact timing can be maintained in the absence of data. The price paid for this independence from data is that there is less power allocated to the commands.

Viking

The Viking Command Detector derives bit timing from transmitted data and is data dependent requiring some transitions over a reasonable span of time. However all the available power in the command channel can be applied to transmission of the commands.

1.2.2 Mariner 69 Command Signal Modulation

The Mariner 69 detector design was constrained by the following command signal characteristics:

1) Use of a two channel system - one channel for bit synchronization and one channel for command data.
2) Frequency and phase coherency between the bit timing and subcarrier frequencies.

The input signal to the unit is given as $PN \oplus F_S \pm \sin 2\pi f_s t + N(t)$ where:

PN = a PCM NRZ pseudo-random noise signal

N(t) = additive noise

F_S = a squarewave subcarrier of frequency f_s

f_s = frequency of a sinewave subcarrier

$\oplus$ = "exclusive or" operation

SNR = 16.5 dB/1 Hz

A "one" is defined as a subcarrier phase of $+ \sin w_s t$ and a "zero" is defined as $- \sin w_s t$. In addition the command bit transitions are coincident with the zero crossings of the sinewave subcarrier. The bits in the PN signal are timed from the same source which generates the subcarrier frequency. The rate of occurrence of PN bits is equal to $2F_S$, where F_S is the subcarrier frequency. The PN bits are then converted to a PCM Bi-Phase format and then added linearly to the subcarrier signal.

The modulated subcarrier signal is generated by multiplying the subcarrier - (a sine wave at f_s) with the NRZ command bits - the modulated subcarrier signal then has the form $D(t) \sin w_s t$ where D is ± 1.*

1.2.3 Mariner 69 Command Detector Abbreviated Theory of Operation

The Mariner 69 Command Detector employs a squaring loop to recover $2F_S$. $2F_S$ is then divided by two to recover F_S. Since the bit timing and subcarrier frequencies are coherently related the bit timing frequency is known as soon as the subcarrier loop has locked onto $2F_S$.

The remaining uncertainty is the phase relationship between the transmitted command bit timing and the recovered bit timing. To reduce this uncertainty a comparison is made between the transmitted PN signal and a stored replica in the Command Detector. The internal PN code is shifted 1 PN bit per code cycle until a match is achieved. The PN cycle length is equal to a command bit period and the resolution in bit timing is limited to $\pm$ one PN bit or one period of $2F_S$.

Power must be transmitted in the sync channel in order for this system to operate - consequently for a power limited composite channel the command signal cannot be allotted all the available power.

1.2.4 Viking Lander Command Signal Modulation

The Viking Lander Command Detector (VLCD) design was constrained by the following command signal characteristics:

---

*Defining a transmitted "1" as + sin $w_s t$ and resetting the recovered subcarrier at the beginning of each bit, to + sin $w_s t$ (or a positive going square wave) eliminates the data or data bar ambiguity. This strategy is not used in the Viking CD, "1" could be $\pm$ sin $w_s t$. In Viking - data or complemented data can be recovered. The problem of deciding on D or $\overline{D}$ is left to the GCSC.

1) Use of a single channel for command transmission.

2) No requirement for coherency between the subcarrier and bit timing frequencies and phase.

The input signal to the Command Detector will be $M_c(t) = V_D(D(t)) \sin (2\pi f_s t + \theta) + N(t)$ where:

V_D = peak voltage of the command subcarrier

θ = arbitrary phase angle

f_s = frequency of the subcarrier (sine wave)

$D(t)$ = the normalized command data signal, + 1 or - 1.*

$N(t)$ = additive noise

SNR = 11.5 dB/4 Hz

Since no power is allocated to a separate synchronization signal - all timing must be derived from the modulated subcarrier described above.

1.2.5 Viking Lander Command Detector (VLCD) - Abbreviated Theory of Operation

Subcarrier recovery is accomplished by means of a squaring loop similar to the Mariner 69 CD. The recovered subcarrier is then used to synchronously demodulate the incoming modulated subcarrier thereby recovering the NRZ command bits (corrupted with noise). The noisy NRZ is fed to a matched filter and a transition tracking loop (TTL). The TTL makes an estimate of the transmitted transition location and supplies this estimate of bit sync to the matched filter (an integrate and dump circuit as in Mariner 69) where the bits are detected. The estimate of where the transition is located is made by integrating across the expected transition location. If the actual transition is not located centrally in the integration interval then a net

*A data "1" may be $\pm \sin (w_s t + \theta)$. Therefore, data or its complement may be recovered.

non zero voltage will result at the end of the integration interval. The noise will add a contribution to the integrated output and will be reflected as a phase perturbation (jitter) on the recovered bit timing. The amount of noise induced jitter will be affected by the amount of filtering used after the integrator. At present a digital implementation of a feed-through plus integrator (lead-lag filter) follows the integrator. The output of the filter is used to determine the countdown ratio of a programmable divider. The Viking Command Detector breadboard bit timing recovery circuits can be viewed as a second order phase lock loop when there are transitions present. Behavior in the absence of transitions is more complex and cannot be easily described without going into more detail. More will be said about the performance of the Viking Command Detector as a function of transition density later in the report.

2.0 SYSTEM DESCRIPTION

2.1 General

This section of the report describes the details of the breadboard command detector system operation. The theory of operation for the subcarrier and bit timing recovery loops, subcarrier presence and bit lock indicators are described. The major specification requirements have been discussed in reference 1 cited previously. In some cases due to clarification in requirements and the results of breadboard testing the original circuit specifications as described in ref. 1 have changed. Where changes have occurred, a discussion of the change is included.

2.2 Subcarrier Recovery

The VLCD as shown in Fig. 2-1 (overall block diagram) uses a squaring type loop to recover the subcarrier frequency. The loop parameters were originally established by an earlier study (see ref. 1) but have undergone some modification since that time.

2.2.1 Loop Noise Bandwidth B_{L_o}

The noise bandwidth of the subcarrier loop was originally designed to be B_{L_o} = .4 Hz (2 B_{L_o} = .8 Hz) where B_{L_o} is the threshold bandwidth. In this case, noise bandwidth is defined as in references 1 and 3 and is the "low pass" equivalent noise bandwidth which must be doubled when loop SNR is calculated as for example:

$$SNR_L = SNR_i \frac{B_i}{2B_L}$$

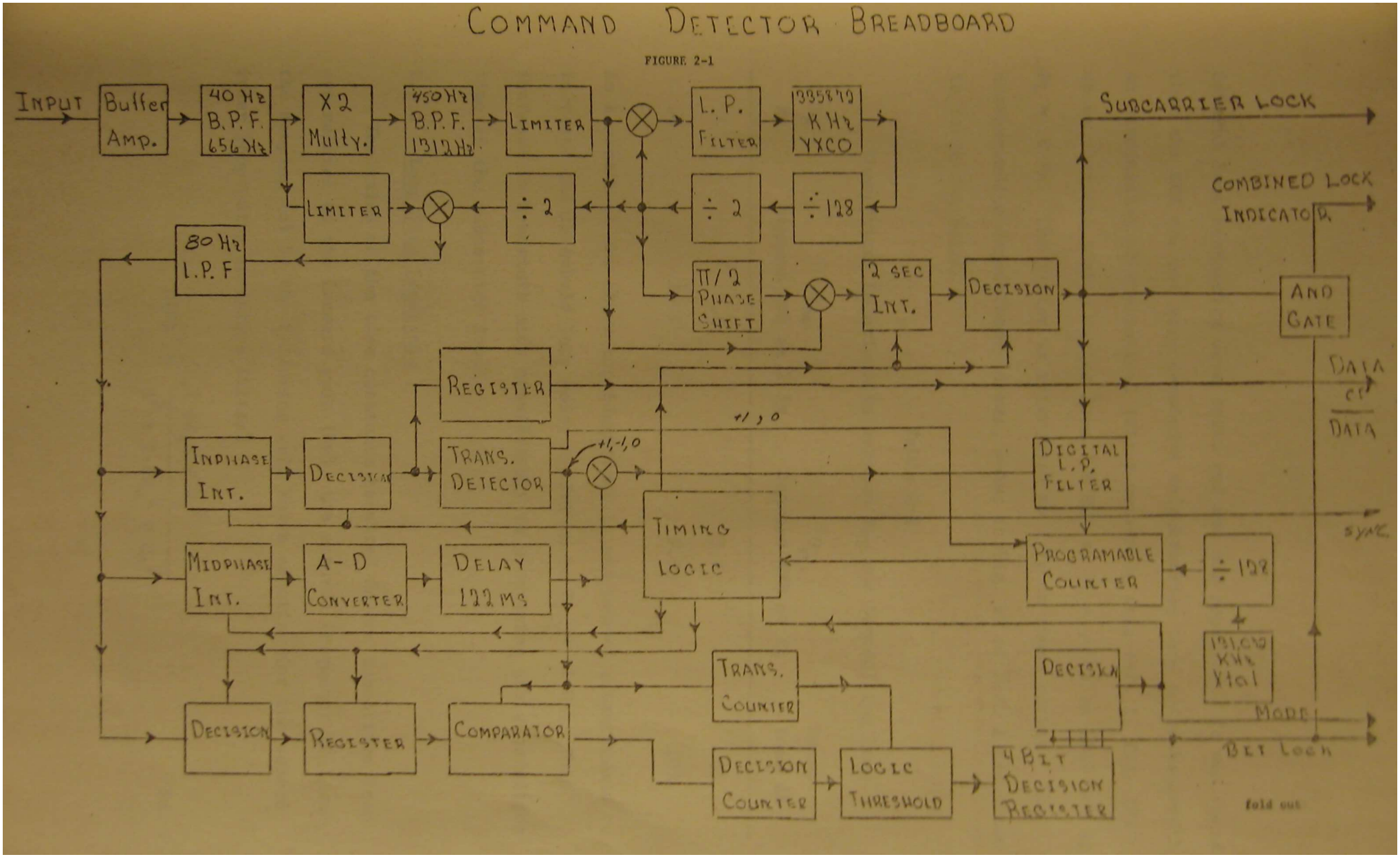
Threshold B_{L_o} is the noise bandwidth in the loop when the threshold signal (E/N_o = 11.5 dB) is applied.

---

1. Op cit.
3. Floyd M. Gardner, "Phase Lock Techniques," p. 20.

COMMAND DETECTOR BREADBOARD

FIGURE 2-1



Several loop bandwidths were tried and the BER measured. It was found that the BER was not very sensitive to subcarrier loop noise bandwidth. An examination of theoretical jitter versus B_L (see ref. 1, Fig. 13) shows that the jitter varies from 7.6 RMS at B_L = .4 Hz to 10.7 RMS at B_L = .8 Hz. The jitter is referenced to 2 F_S in these curves. The corresponding demodulator losses, shown in Fig. 12 of ref. 1 are shown in Table 2-1 below.

Table 2-1

Theoretical Relationship between B_{L_T} and Demodulator Loss

B_L Hz	θ_{no} Degrees RMS at 2 F_S	θ_{no} Degrees RMS at F_S	Demod. Loss dB
.4	7.6	3.8	.01
.8	10.7	5.35	.03

As a result of the above considerations it was deemed advantageous to increase the threshold loop noise bandwidth to B_{LT} = .8 Hz. This increase in bandwidth aids considerably in shortening the acquisition time of the subcarrier loop.

2.2.2 Loop Time Constants

The value of the time constants required in the subcarrier loop are related to the forward gain (Kv), the natural frequency (W_n) and the damping (d) by the following well known equation for the second order loop using an active filter:

$$H(S) = \frac{2\,dW_n S + W_n^2}{S^2 + 2\,dW_n^2 + W_n^2} \qquad \text{Eq. 1}$$

where $W_n = \sqrt{\frac{Kv}{\tau_1}}$ Eq. 2

$d = \frac{\tau_2}{2}\sqrt{\frac{Kv}{\tau_1}}$ Eq. 3

It was desired that the time constants should be based on a threshold loop noise bandwidth of B_{L_o} = .8 Hz. The calculation of τ_1 and τ_2 is presented:

d_T	damping factor at threshold
W_{n_T}	natural frequency at threshold
K_{v_T}	forward gain at threshold
α	limiter suppression at threshold
$(SNR_i)_T$	signal to noise at limiter output at threshold

choosing: $d_T = \frac{1}{\sqrt{2}}$

given: $2\ B_{L_o}$ = 1.6 Hz (see section 2.2.1)

K_{v_T} = 21/sec (reference 1)

$(SNR_i)_T$ = -3.2 dB (reference 1)

K_{v_T} is derived from an assumed frequency offset of $\pm$ .01% and a design point assumption that the static phase error be less than .1 times the 3 σ value of the loop phase jitter (at 2 F_S) -see reference 1.

The frequency offset requirement has since been increased to $\pm$ .04%. The static phase offset is now, for the breadboard,

$$\theta_{STATIC} = \frac{\Delta W}{K_{v_T}} = \frac{2\pi\ (4\times10^{-4})\ 1.300\times10^{3}\ Hz}{21}$$

$\theta_S = 1.55\times10^{-1}$ radians = 8.9^{o} @ 2 F_S

The value of K_{v_T} in the breadboard was not changed to accommodate the increased frequency offset therefore the static offset of 8.9^{o} is

experienced in the breadboard for the .04% frequency offset case.

α_T = .53 (for -3.2 dB SNR at input to limiter).

K_{VSS} (strong signal) = $K_{VT}/\alpha = \frac{21}{.53} = 39.7/\text{sec}$

and from

$$\frac{B_{L_T}}{W_{n_T}} = \frac{1}{2}\left(d_T + \frac{1}{4d_T}\right)$$

$$\frac{B_{L_T}}{W_{n_T}} = .53$$

$$W_{n_T} = \frac{B_{L_T}}{.53} = \frac{.8 \text{ Hz}}{.53} = 1.51 \text{ rad/sec}$$

consequently

$$W_{n_T} = \sqrt{\frac{Kv}{\tau_1}}$$

$$1.51 \text{ rad/sec} = \sqrt{\frac{21}{\tau_1}}$$

$$\tau_1 = \frac{21}{(1.51)^2} = 9.23 \text{ sec}$$

$$\tau_2 = \frac{2\ d_T}{\frac{Kv}{\tau_1}} = \frac{2\ d_T}{W_{n_T}} = \frac{1.414}{1.51}$$

$$\tau_2 = .933 \text{ sec}$$

These time constants are implemented in the subcarrier phase lock loop with an active lag-lead filter. The details of the design are covered in another section of this report.

Table 2-2 is a summary of the system parameters which affect the design of the subcarrier phase lock loop.

Table 2-2

Summary of Subcarrier Recovery System Parameters

Parameter	Value*	Comments
SNR into Doubler	(+1.3 dB/40 Hz)	ref. 1
SNR out of Doubler	(-3.2 dB/40 Hz)	ref. 1
SNR out of Limiter	(-3.1 dB/ Hz)	ref. 1
Post Doubling BPF Bandwidth	(450 Hz/3 dB)	Minimum Q for smallest phase shift due to filter aging
B_{L_T} Loop Noise Bandwidth	(.8 Hz)	(Low pass equivalent)
Oscillator Stability†	(± .01%)	VCXO used.
DC Gain	(21/sec)	For ± .01% freq. offset see ref.
Loop SNR at Threshold	(10.9 dB/1.6 Hz)	$\text{SNR}_{\text{Loop}} = -3.1 \text{ dB} + 10 \log \frac{40 \text{ Hz}}{2 B_{L_T}}$
Limiter Suppression α	.53	
Acquition Time†	(8 secs) (TBS)	(For ± .01% offset) (For ± .04% offset)

*Calculated for threshold inputs and end of life

†Specification requirement