SH-1 Embedded Workhorse User Manual

Version 1.0

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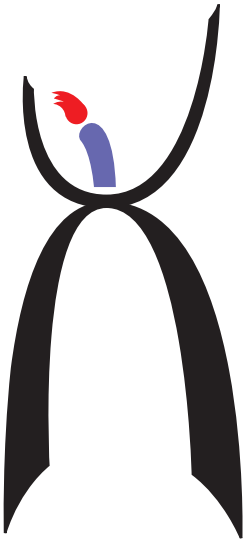
Xtreme Ideas Technology Development



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1 Feature Summary

- 12 MHz Hitachi Super-H 32-bit RISC engine
- 8 MB of Fast-Page DRAM
- 128K of battery-backed SRAM
- 1 MB of in-circuit programmable FLASH
- 8K of fast SRAM (user-managed cache)
- Y2K compliant real-time clock
- eight 10-bit A/D channels with S/H, 11.2 us conversion time
- two 12-bit D/A channels, 14 us settling time
- up to 5 hardware PWM channels
- up to 20 digital outputs
- up to 10 digital inputs
- up to 5 hardware interval counter channels (for shaft encoders, tachs, etc.)
- hardware programmable timing pattern generator
- two RS-232 serial ports (up to 250Kbaud)
- watchdog and wakeup timers
- power supply monitor protects against data corruption during power dropouts
- high-efficiency switching regulator
- input voltage range from 3.8V to 13V
- drop-in solution compatible with many battery chemistries
- low power—less than 100 mA typ., < 2 mA sleep, plus zero-power shutdown mode
- easy to use vertically stacking expansion bus
- built-in temperature sensor
- low profile—7 mm minimum board-to-board clearance in vertical stack
- tiny 2.02” x 3.2” footprint (smaller than a credit card)
- programming support with popular and free GNU tools

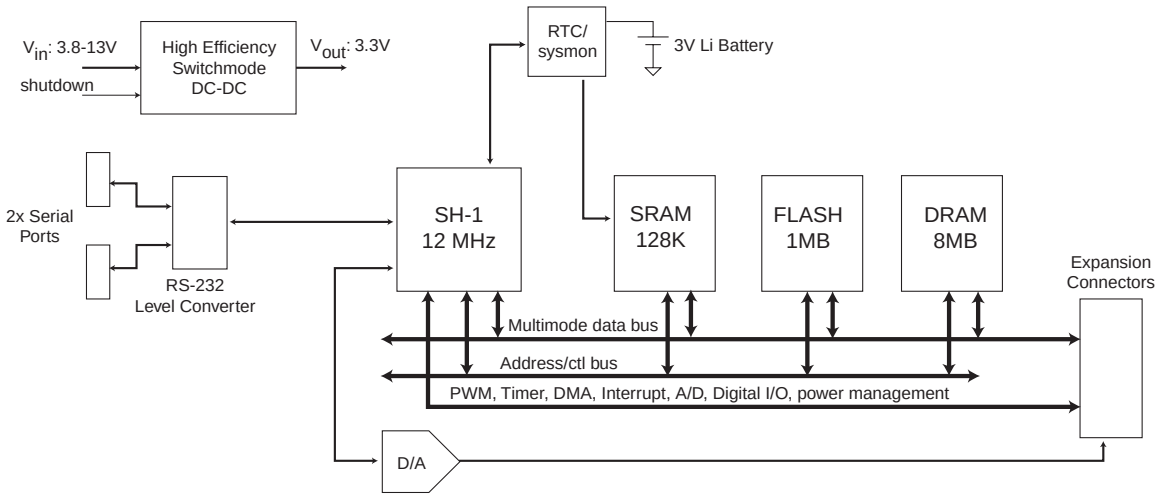

Figure 1: SH-1 Workhorse system block diagram

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Descriptive Specifications

2.1 Power Supply

The SH1EW can be powered from one of two sources, but never by both at the same time.

2.1.1 Powering via unregulated power input

There are two possible points for attaching unregulated power. One may either provide power through the expansion headers, or by directly soldering wires to the board. A square pad in the southwest corner of the board, labeled V_{in}, is the positive input; the reverse side has a pad for the GND input.

The unregulated input voltage may continuously range from 3.8V to 13V. Input voltages can be as low as 3.3V; the 0.5V margin is specified to enhance noise immunity. The board is PTC fuse limited to 750 mA on this input, and it has reverse voltage protection. Any power source connected to the board should be specified to provide up to 500 mA peak current.

When powered off of the unregulated power input, a small amount of power may be tapped off of the regulated power output for a convenient source of 3.3V. The regulator on the SH1EW is specified to provide up to 600 mA total power.

2.1.2 Powering via regulated power input

There is a pair of pads on the east side of the board for attaching regulated 3.3V power. The 3.3V pad is on the top side; the GND pad is on the bottom side. Power provided at this input should be regulated to 3.3V ± 5% @ 500 mA peak. Use caution when connecting power to this input, as there is no fuse or reverse voltage protection on this input.

2.2 Serial Interface

The SH1EW has two serial ports available off of J1. It is a 6 pin HRS DF3-style connector, with the mating HRS part number DF3-6S-2C; the socket crimp pins (required by the mating connector) are HRS part number DF3-2428SC. They are readily available through Digi-Key (connector: H2087-ND, socket pins: H2138-ND) for under $3.

The voltage levels are RS-232 compliant, and the baud rate is user programmable. The nominal rate is 38.4Kbaud, but the internal baud rate generator can be cranked up to 250Kbaud.

Please refer to Figure 2 and Table 1 for connector pinouts.

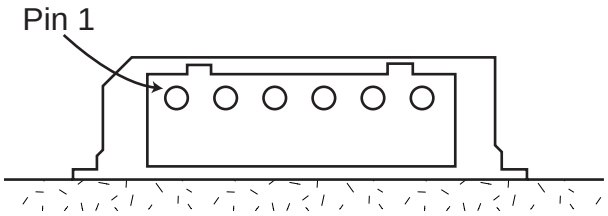


Figure 2: Serial Connector (J1) pin 1 orientation (viewed head-on from side of board)

Pin	Function
1	GND
2	TxD1 (data out of board)
3	RxD1 (data into board)
4	GND
5	TxD2
6	RxD2

Table 1: Serial connector (J1) pinout

2.3 Expansion Connectors

2.3.1 Physical Specifications

There are two pairs of expansion connectors on the SH1WH. They are positioned to allow the vertical stacking of peripheral cards such as break-out boards (SH1WH-BB1) and high-current motor driver cards (SH1WH-MD1). The connector pinouts are designed to allow any card to be stacked above or below any other card.

The connectors are Harwin part numbers M60-6162022 (plug, top: J2 and J4) and M60-6042022 (socket, bottom: J3 and J5). They are available directly through Harwin ((812)285-0055) or its distributors for about $2 per connector. These particular connectors configure the SH1WH for a nominal board-to-board clearance of 7 mm, although if additional clearance is desired, a taller connector on the mating board may be chosen for a total clearance of 9 mm.

All of the I/O signals except for the serial I/O are accessed via these connectors. This solution was chosen so users can design their own low-profile application card for space-conscious applications, but can still break the signals out to convenient 0.1” spaced double-row headers for prototyping via an inexpensive break out board such as the SH1WH-BB1.

Connector pinouts and diagrams are available in Figure 3, Figure 4, and
Figure 5. Orientation nomenclature is as follows: “north” is the top of the board when viewed so that the silkscreen is in normal reading orientation. “West” is the left hand side of the board when looking at the side with the switches and high-profile components (this is usually referred to as the “top” side). Likewise, “east” is the right hand side of the

board. When looking at the back of the board, west and east are reversed, so west is on the right and east is on the left.

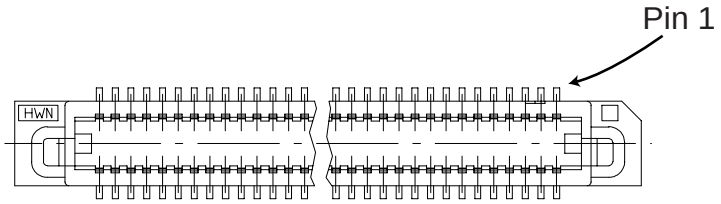


Figure 3: J2 and J4 pin 1 location, top view of connector

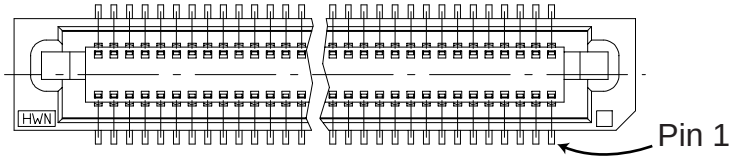


Figure 4: J3 and J5 pin 1 location, top view of connector

West Connector
Top View

Vbatt	1	40	PGND
Vbatt	2	39	PGND
Vbatt	3	38	DGND
Vbatt	4	37	AD0
CLK	5	36	AD1
DGND	6	35	AD2
RES	7	34	AD3
RD	8	33	AD4
WR	9	32	AD5
CS6	10	31	AD6
CS7	11	30	AD7
A0	12	29	DGND
A2	13	28	A1
A4	14	27	A3
A6	15	26	A5
DGND	16	25	A7
PA14	17	24	PA15
PA12	18	23	PA13
NC	19	22	PA11
NC	20	21	DGND

East connector
Top View

AVrefI	1	40	AGND
AN7	2	39	AN6
AN5	3	38	AN4
AN3	4	37	AN2
AN1	5	36	AN0
AVRefO	6	35	Aout0
Aout1	7	34	AGND
DGND	8	33	DGND
Vutil	9	32	NMI
shutdwn	10	31	wake out
PWM0	11	30	PWM1
EN0	12	29	EN1
DIR0	13	28	DIR1
PWM2	14	27	PWM3
EN2	15	26	EN3
DIR2	16	25	DIR3
DGND	17	24	DGND
PWM4	18	23	AH/samp
EN4	19	22	NC
DIR4	20	21	NC

Figure 5: Connector pinouts. The west connector has primarily high current and noisy signals; the east connector has primarily quiet signals. Note that connector pinouts are identical on the top and the bottom.

2.3.2 Signal Specifications

2.3.2.1 Direct Processor Bus Signals

AD[7:0] *I/O* Multimode address and data bus. Depending on access location, this bus may behave either as a multiplexed address/data bus or as just a data bus. This bus may also be treated as either a simple 8-bit bus or the lower byte of a 16-bit wide bus.

A[7:0] *O* Address bits from the processor

RD *O* Read enable from the processor, active low

WR *O* Write enable from the processor, active low

CS7 *O* Chip select from the processor, active low. This CS line corresponds to 8-bit accesses with an unmultiplexed bus mode in addresses from 0x7000000 to 0x7FFFFFF.

CS6 *O* Chip select from the processor, active low. This CS line corresponds to 8 or 16-bit wide accesses in a multiplexed address/data bus mode in addresses from 0x6000000 to 0x6FFFFFF; if the 14th address bit is high, then the bus behaves as if it were 16 bits wide; if it is low, then the bus behaves as if it were 8 bits wide. It also corresponds to 16-bit accesses in an unmultiplexed bus mode in addresses from 0xE000000 to 0xEFFFFFF.

RES *I/O* Hard reset, active low. This signal is debounced and pulled low for 250 ms on any of the following conditions: reset button depressed, Vcc out of range (2.88V typ.), power-on reset, or watchdog timer time-out (if enabled). A hard reset will clear processor state and is required to wake up out of deep-sleep modes. RES is a wired-AND signal, so users may pull RES low to force a reset condition.

CLK *O* 12 MHz clock signal, synchronous to direct processor bus signals

NMI *O* Non-maskable interrupt output. This signal is triggered when the alarm clock in the RTC times out, or when the user depresses the NMI button.

AH/samp *I/O* Software configurable pin to either address hold output or A/D sample trigger input. Address hold is used when the expansion bus is in multiplexed address/data mode. A/D sample trigger is optional as the sample trigger can be set by software as well.

2.3.2.2 Digital I/O

PA[15:11] *I/O* Programmable function digital I/O ports. In addition to simple digital I/O, PA[15:12] can also be remapped in software to function as active-low interrupt lines or DMA handshaking lines; PA11 can be remapped to function as a timing pattern generator output.

PWM[4:0] *I/O* Pulse width modulation control output. Dedicated hardware drive these lines with square waves of varying duty cycles; properties of the PWM output are set by software. These signals can also be configured to function as digital I/O, timing pattern generator outputs, or as interval timer inputs.

EN[4:0] *O* Dedicated digital outputs. While the label may suggest that it can be used to enable motors under PWM control, this output may be used for any function. EN[4:0] maps to bits 4:0 of any data written to locations ranging from 0xA000000 through 0xAFFFFFF.

DIR[4:0] *O* Dedicated digital outputs. While the label may suggest that it can be used to set the direction of motors under PWM control, this output may be used for any function. DIR[4:0] maps to bits 12:8 of any data written to locations ranging from 0xA000000 through 0xAFFFFFF.

2.3.2.3 Analog Signals

AN[7:0] *I* Input to A/D converter. The A/D converter is a 10-bit SAR type converter.

Aout[1:0] *O* Output of D/A converters. The D/A converters have 12-bit resolution.

AVrefI *O* Reference voltage used by the A/D converter. This AGND-referenced voltage represents the maximum voltage that the A/D converter can sample. Excessive current draw from this output will affect A/D converter accuracy.

AVrefO *O* Reference voltage used by the D/A converter. This AGND-referenced voltage represents the maximum voltage output by the D/A converter. Excessive current draw from this output will affect D/A converter accuracy.

AGND *PWR* Analog ground. This is an isolated, low-current return path for analog signals.

2.3.2.4 Power Control

shutdwn *I* A high input on this pin causes the switching regulator to shut down, effectively turning the board off. This input is internally tied low with a 10K resistor.

wakeout *O* This is an alarm clock output that functions regardless of the state of Vcc. Its polarity and trigger time is programmable. It is internally connected to the NMI of the processor.

2.3.2.5 Power

Vutil *NC* This is a utility voltage pin provided on the expansion headers for use by expansion cards. It is not connected on the SH1WH.

DGND *PWR* Digital signal ground.

PGND *PWR* Power ground; high current return path for system power.

Vbatt *PWR* System power. Nominally provided by a battery, but any unregulated DC input between 3.8 and 13V is acceptable.

2.3.2.6 Miscellaneous

NC *NC* Internally not connected. For use by expansion cards.

2.4 Miscellaneous Test Points

The SH1WH is equipped with a few test points to aid debugging. The important test points are highlighted in gray in Figure 6 and Figure 7. The PCLK test point has the same signal as the CLK pin in the expansion header. GND and 3.3V test points are tied to the internal power and ground planes. The SP0 and SP1 pads are connected to SH-1 pins that can either be software configured to be simple I/Os or auxiliary PWM, interval counter, or timing pattern generator I/Os.

Wires are attached to test points either by probe contact or soldering.

2.5 Temperature Sensor

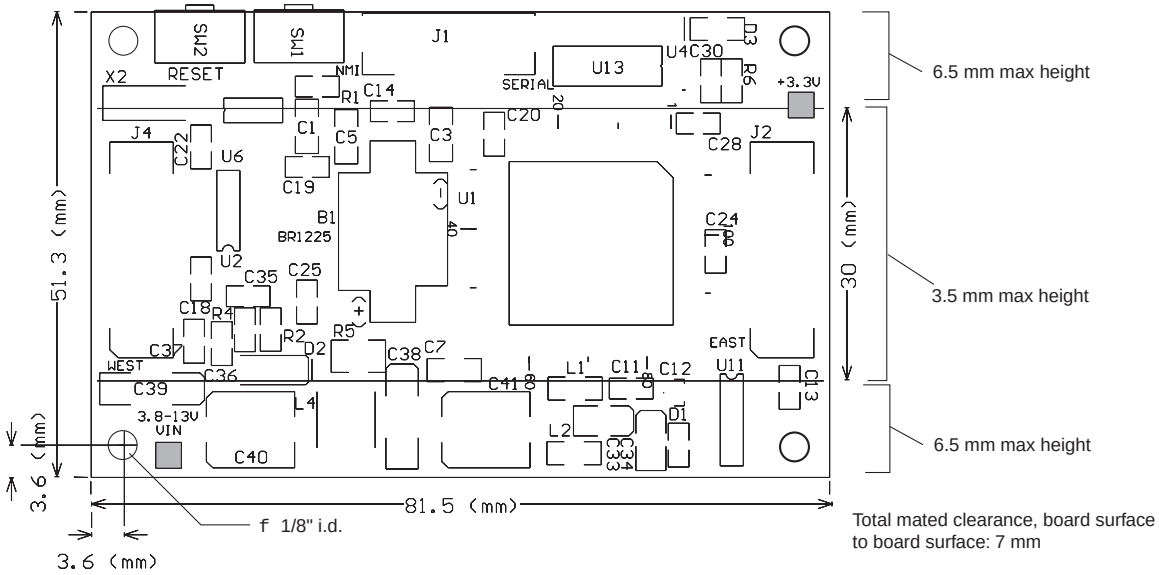
The SH1WH has a built-in temperature sensor for detecting the ambient operating temperature near the center of the bottom side. It is provided for the detection of hazardous thermal conditions on peripheral cards, such as motor driver cards. The sensor itself is accurate to ± 3°C and is sampled by an 8-bit A/D converter.

2.6 Diagnostic LED

The SH1WH has a single green LED for diagnostic purposes. This green LED is internally connected to the SP1 test point. For power conscious applications, this LED should be removed or left off at all times.

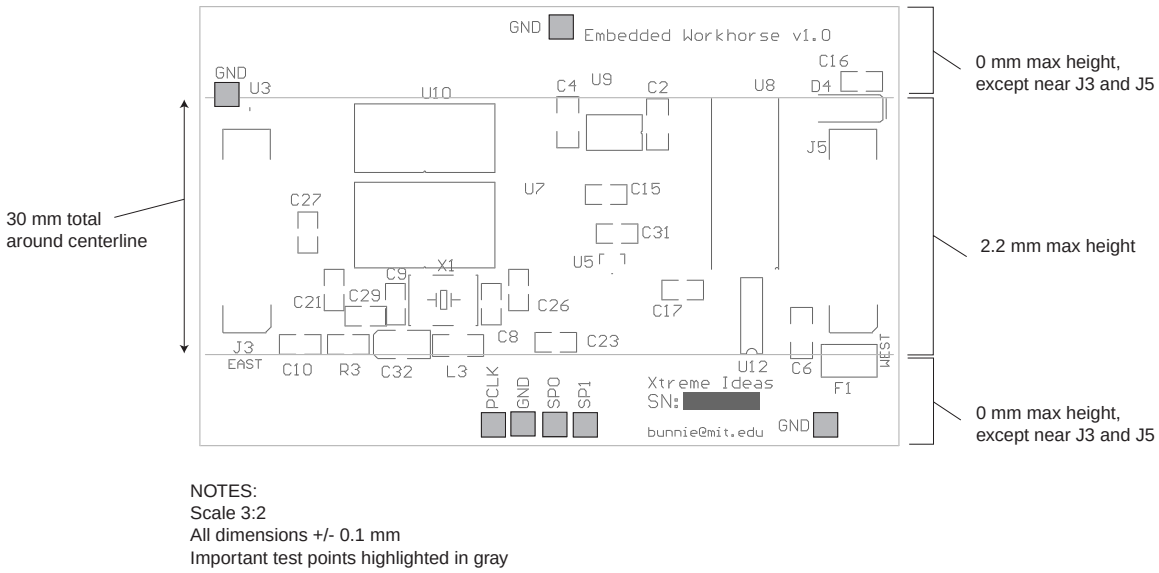
2.7 Physical Dimensions

Figure 6 and Figure 7 illustrate the dimensions of the SH1WH board. Note that there are strict regulations as to the maximum height of components on different regions of the board. A region about 10 mm wide on the north and south sides of the board are reserved for top-populated high-profile components (up to 6.5 mm tall). In order to accommodate this provision, no components are allowed to be populated within 10 mm of the north and south sides on the bottom side of the board. The 30 mm strip centered about the middle of the board has the 7 mm board-to-board clearance evenly distributed between the top and the bottom sides, at 3.5 mm per side. Mating cards should keep these restrictions is mind.



NOTES:
Scale 3:2
All dimensions within +/- 0.1 mm
Important test points highlighted in gray

Figure 6: Top silkscreen and physical dimenions



NOTES:
Scale 3:2
All dimensions +/- 0.1 mm
Important test points highlighted in gray

Figure 7: Bottom silkscreen and physical dimensions

2.8 Memory Map

The SH1WH has several memory-mapped peripherals. A general memory map is provided in Figure 9.

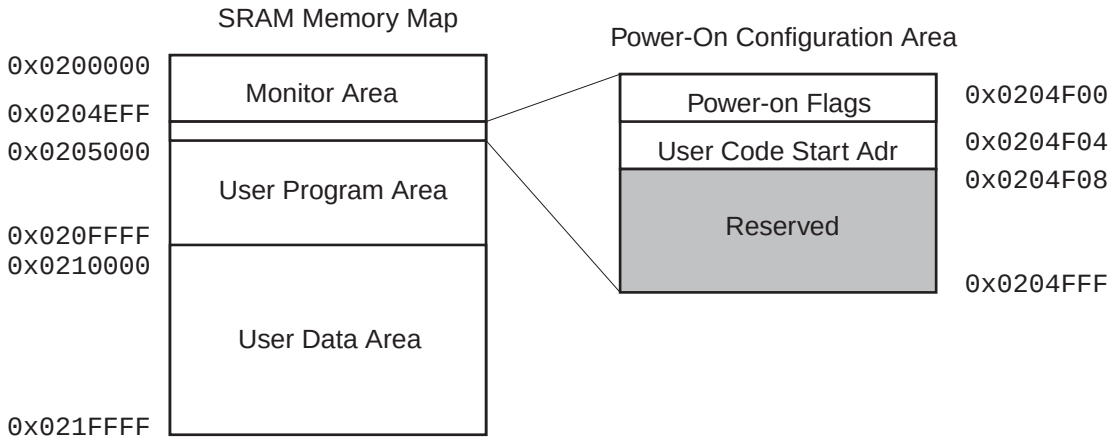


Figure 8: Recommended SRAM footprint.

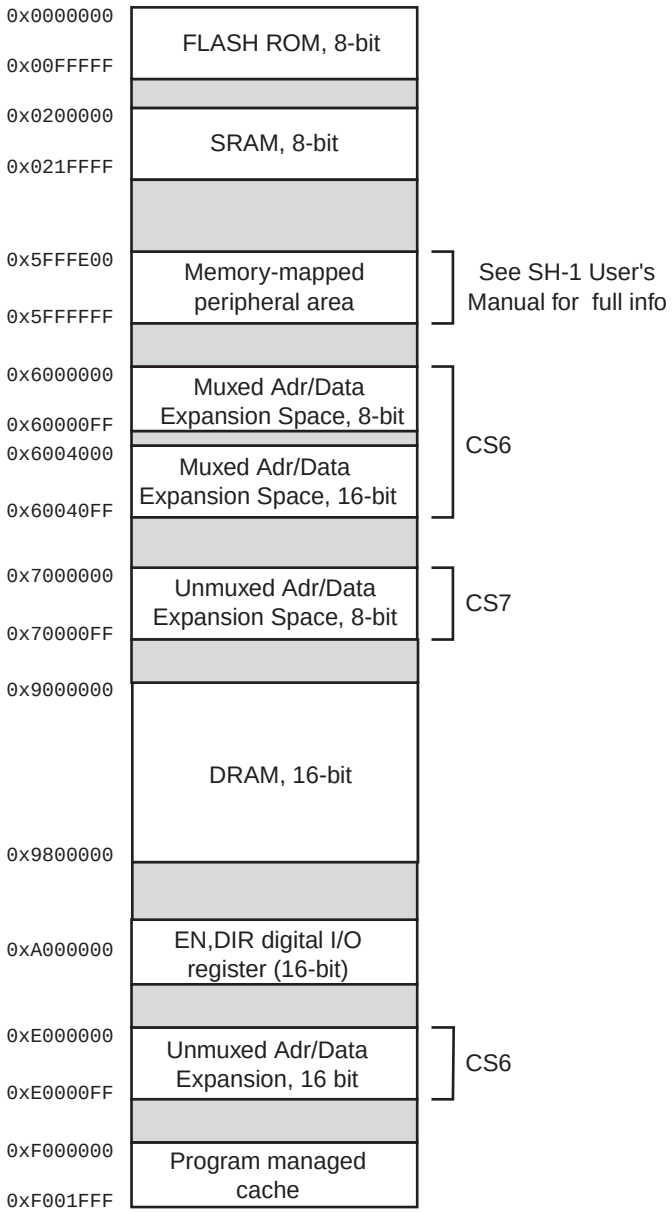


Figure 9: SH1WH memory map. Note that gray areas should *not* be accessed at any time. The memory map is heavily aliased and accesses to gray areas may cause unpredictable behavior.

The SRAM and FLASH ROM spaces also have recommended memory maps; if your application is to be compatible with the monitor, it should use only the free spaces designated in the memory maps of Figure 10 and Figure 8.

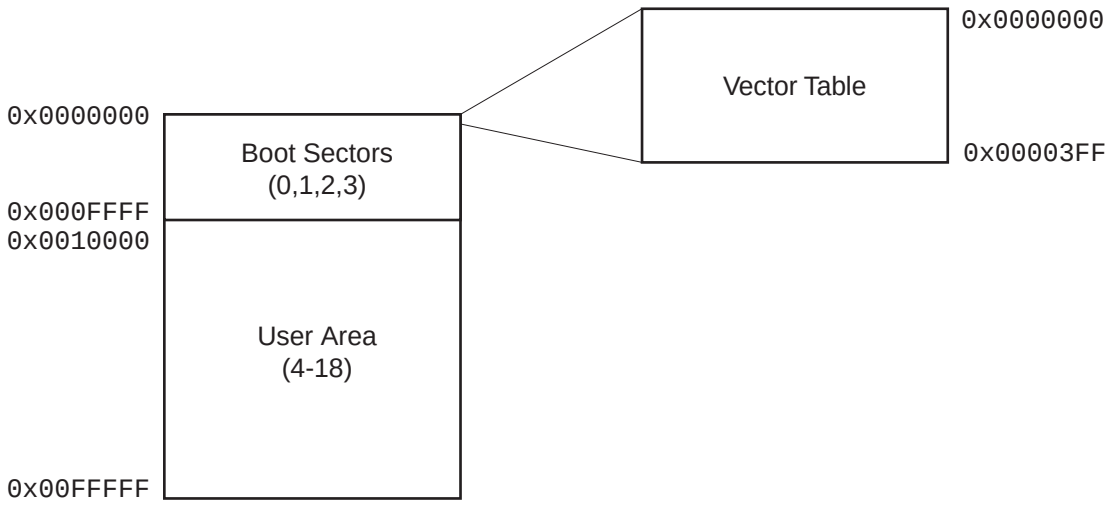


Figure 10: Recommended FLASH ROM footprint.

3 Quantitative Specifications

3.1 Absolute Maximum Ratings

Voltage on Vbatt relative to PGND	-0.3V to 13V
Voltage on +3.3V input relative to DGND	-0.3V to 4.6V
Operating Temperature, T_A (ambient)	0° C to 70° C
Storage Temperature	-55° C to 125° C

3.2 DC Specifications

3.2.1 Power Supply

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
Unregulated supply voltage	VBATT	3.3		13	V	1
Regulated supply voltage	VCC	3.14	3.3	3.45	V	
Power supply current, normal operating mode	ICC		100	350	mA	
Power supply current, sleep mode	ISLEEP		2		uA	
Standby voltage	VSTBY	2.5			V	
VCC reset protection trip threshold	VTRIP	2.80	2.88	2.97	V	
VCC switchover to battery backup threshold	VBBACK	2.62	2.70	2.78	V	

3.2.2 Digital I/O

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
Input high voltage, VCC = 3.3V	VIH	2.3		3.6	V	
Input low voltage, VCC = 3.3V	VIL	-0.3		0.66	V	
Input leakage current, EN[4:0], DIR[4:0]	IILED			5	uA	
Input leakage current, all other inputs	IIL			1	uA	

Output high and low current, EN[4:0], DIR[4:0]	IOED			24	mA	
Output high current, all other outputs	IOL			2	mA	
Output low current, all other inputs	IIL			10	mA	
Output high voltage, VCC = 3.3V, IOH = 1 mA	VOH	2.6			V	
Output low voltage, VCC = 3.3V, IOL = 2 mA	VOL			0.6	V	
Input capacitance	CI		30		pF	

3.2.3 Analog I/O

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
A/D resolution			10		bits	
A/D reference voltage	VREFI		2.50		V	
A/D ref voltage tolerance, IREFI = 0				±21	mV	
A/D ref maximum output current	IREFI			0.1	mA	
A/D minimum input voltage	VADL	-0.3	0		V	
A/D maximum input voltage	VADH		2.5	3.3	V	
A/D input current	IADI		1.0		uA	
D/A resolution			12		bits	
D/A reference voltage	VREFO	1.19	1.22	1.25	V	
D/A ref maximum output current	IREFO			0.1	mA	
D/A output voltage, code = 0x000	VDAL		0		V	
D/A output voltage, code = 0xFFF	VDAH		2.50		V	2
D/A output current	IDAO		70		mA	

3.3 AC Specifications

3.3.1 Processor Expansion Bus

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
CLK rise and fall time	TCRF		10		ns	
CLK frequency	TCFREQ		12.0		MHz	
IRQ, NMI setup time	TINTS	160			ns	
RES pulse width	TRESPW	1.7			us	

Please refer to the “Hitachi SH7032/7034 Hardware Manual” for detailed specifications of the processor expansion bus timings. The SH-1 is a highly programmable part and thus the timing explanations can be quite elaborate.

3.3.2 Analog AC Performance

Conditions: T_A = -20 to 75 °C, AVcc regulated to within ±10%.

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
AD converter external trigger start delay time	TTRGS	50			ns	
AD converter time	TCONV		11.2		us	
AD nonlinearity error				±4.0	LSB	
AD offset error				±4.0	LSB	
AD full-scale error				±4.0	LSB	

AD quantization error				±0.5	LSB	
AD absolute accuracy				±6.0	LSB	
DA converter output slew rate, 100 pF || 5K load		0.5	1.0		V/us	
DA converter settling time			14		us	
DA digital feedthrough			0.3		nV•s	
DA integral nonlinearity error			±2.0		LSB	
DA differential nonlinearity error				±0.5	LSB	

3.3.3 Temperature Sensor

Parameter/Condition	Symbol	Min	Typ	Max	Units	Notes
Sensor inaccuracy from –25 to 125 °C				±3	°C	
Output voltage at 0 °C			424		mV	
Sensor slope			6.25		mV/ °C	
A/D converter resolution			8		bits	
A/D full-scale voltage			2.55		V	
A/D Differential nonlinearity			±0.5		LSB	
A/D conversion time			488		us	

Notes:

1. For applications involving 12V lead-acid battery chemistries, it is recommended to put at least three diode drops between the battery and the SH1WH because lead-acid batteries often charge at voltage above 14V.
2. There is a 2x gain stage on the output of the DAC, which is referenced to VREFO.

4 Applications Information

4.1 Basic Usage

The SH1WH is capable of operating in both stand-alone and host modes. The default setting is for host mode operation; users may select host mode or stand-alone mode on bootup by setting bit 0 at location 0x204F00 to 0 or 1, respectively.

4.1.1 Booting

In host mode, the SH1WH runs an interactive monitor which is pre-loaded into the FLASH ROM. The interactive monitor has provisions for checking and setting memory locations, copying blocks of data, uploading data, changing the program counter, and programming the FLASH ROM.

Thus, the intended application development cycle consists of writing the code of the host machine, uploading it to SH1WH RAM, and testing it. Once the code is tested, the user has two options. The user may recompile the code to link in the interrupt vector tables and basic initialization routines and burn that over the existing boot code, thus destroying the code for host mode (not recommended). The other option is that the user may simply copy the code into one of the data sectors of FLASH ROM and set a pointer to it in the

battery-backed SRAM at location 0x204F04, and toggle the host/stand-alone mode bit in the SRAM. The next time the system is rebooted, it will complete the built-in initialization sequence and jump to the user code; if interaction in host mode is desired at any time, the user may depress the RESET button while holding down the NMI button to force a reboot into host mode.

The default host mode requires a host terminal running at 38400 N-8-1 for interactive operation. The host should be connected to port 2 (TxD2, RXD2, pins 5 and 6 on J1).

5 Appendix: SH-1 Internal Mappings

Table 2 gives the mapping of SH1WH expansion lines to SH-1 signal pins per the "SH7032/7034 Hardware Manual". Table 3 gives the mapping of SH1WH internal lines to SH-1 signal pins per the hardware manual specification. Primary operating mode of SH-1 pin is highlighted in boldface.

SH1WH name	SH-1 pin name	Direction	SH-1 pin number
PWM4	PB4/TP4/**TIOCA4**	O	102
PWM3	PB2/TP2/**TIOCA3**	O	100
PWM2	PB0/TP0/**TIOCA2**	O	97
PWM1	PA10/DPL/**TIOCA1**	O	64
PWM0	PA0/CS4/**TIOCA0**	O	53
SP1	**PB5**/TP5/TIOCB4	O	103
SP0	**PB3**/TP3/TIOCB3	I/O	101
PA15	**PA15**/IRQ3/DREQ1	I/O	69
PA14	**PA14**/IRQ2/DACK1	I/O	68
PA13	**PA13**/IRQ1/DREQ0/TCLKB	I/O	67
PA12	**PA12**/IRQ0/DACK0/TCLKA	I/O	66
PA11	**PA11**/DPH/TIOCB1	I/O	65
AN[7:0]	PC[7:0]/**AN[7:0]**	I	95-92, 90-87
WR	PA4/WRL/**WR**	O	57
RD	PA6/**RD**	O	59
AH/samp	PA9/**AH**/IRQOUT/**ADTRG**	I/O	63

All other signal pin names on expansion bus are identically named in the "SH7032/7034 Hardware Manual", except for EN[4:0] and DIR[4:0], which are driven by an external 16-bit register chip.

Table 2: Mapping of expansion connector signals to SH-1 signals.

The SH1WH has a number of internal signals for interfacing to peripherals such as the RTC and D/A converter that the user should also know about. A brief explanation of the internal signals is as follows.

WDKICK *O* Watchdog kick output. When the watchdog timer function is enabled in the RTC, it is necessary to kick the watchdog timer periodically using this signal to prevent a watchdog reset.

FLASH_RYBY *I* Flash ready/busy input. Used for hardware polling of FLASH ROM embedded algorithm progress for erasing and programming.

ANCLK *O* Clock signal to D/A converter.

ANDIN *O* Serial data to D/A converter.

ANCS *O* Chip select output to D/A converter.

RTCCLK *O* Clock signal to real-time clock chip.

RTCCS *O* Chip select to real-time clock chip.

RTCIO *I/O* Data to and from real-time clock chip.

SER_INV_N *I* Invalid serial data input. Serial line driver automatically shuts down when no valid serial signals are present.

RxD[1:0] *I* Receive data from serial interface.

TxD[1:0] *O* Transmit data to serial interface.

SH1WH name	SH-1 pin name	Direction	SH-1 pin number
WDKICK	**PA7**/BACK	O	60
FLASH_RYBY	**PA8**/BREQ	I	62
ANCLK	**PB13**/TP13/IRQ5/SCK1	O	112
ANDIN	**PB14**/TP14/IRQ6	O	1
ANCS	**PB15**/TP15/IRQ7	O	2
RTCCLK	**PB6**/TP6/TOCXA4/TCLKC	O	104
RTCCS	**PB7**/TP7/TOCXB4/TCLKD	O	105
RTCIO	**PB12**/TP12/IRQ4/SCK0	I/O	111
SER_INV_N	**PB1**/TP1/TIOCB2	I	98
RxD1	PB8/TP8/**RxD0**	I	107
RxD2	PB10/TP10/**RxD1**	I	109
TxD1	PB9/TP9/**TxD0**	O	108
TxD2	PB11/TP11/**TxD1**	O	110

Table 3: Mapping of SH1WH internal signal names to SH-1 signals.

NOTES: