RHP4K User’s Guide
Published by Xtreme Ideas Technology Development
Part number 1007-001-001-X0

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Congratulations and thank you on your purchase of Xtreme Ideas Technology Development’s RHP4K. This user’s guide contains details on how to setup and use your RHP4K.

### Specifications

#### General
- Size: 3.8” x 5.4” (9.6 cm x 13.6 cm)
- Power: +5V DC +/- 10% @ 400 mA nominal

#### Operating Conditions
- Operating Temperature: 0 - 70 °C
- Humidity: 5-95% non-condensing

#### Interfaces
- IEEE1284 parallel port plus scalable network enhancements for primary configuration and host data communications supporting 0.5 MB/s normal maximum transfer rate
- Standard 5-wire serial daisy chain configuration ports for scalable network option
- Proprietary memory expansion port supporting 64K x 16 synchronous SRAM module at up to 66 MHz
- Field programmable clock (FPC) compliant socket supporting two-wire clock programming interface

#### FPGA Support
- Xilinx 4000, 4000A, 4000E series 5V FPGAs in 84-pin PLCC package (4003 to 4010 offered in this package)

#### Clock
- 10 MHz crystal included with device; with FPC upgrade, 391KHz to 100 MHz programmable
Device Diagram

- Power connector
- Node ID select
- Clock test point
- Ground test point
- Memory expansion port
- Clock termination select
- Mode select (top closed = master, bottom closed = slave)
- Fuse
- Daisy chain configuration from master
- Daisy chain configuration to slave
- FPGA
- LED
- User data
- Config done
- Power
- Config data source
- FPGA config mode
- Error mastering
- IEEE1284 centronics parallel connector
- Init
- Clock
- Program
- Power connector
- Config done
- Master mode select (all closed = master)
Port Pin-outs

Power Connector
front view

+5V  GND

Daisy Chain
Configuration Port Pinout
(top view)

CCLK - 1  2 - GND
GND - 3  4 - DIN (to Master) / DOUT (to Slave)
INIT - 5  6 - GND
DONE - 7  8 - PROG

IEEE 1284 Port

NSTROBE - 1
D0 - 2
D7 - 9
NACK - 10
BUSY - 11
END - 12
SEL - 13
AUTO - 14
GND - 17
GND - 18
19 - GND
20 - GND
21 - GND
22 - GND
23 - GND
24 - GND
25 - GND
26 - GND
27 - GND
28 - GND
29 - GND
30 - GND
31 - NINIT
32 - NERR
33 - GND
36 - NSEL

FPC Pinout
(top view)

N.C. - 1
SCLK - 5
SDATA - 6
GND - 7
14 - Vcc
8 - fout

IEEE 1284 Port

Vcc - 1  2 - Vcc
DQ14  DQ15
DQ13  DQ16
DQ12  DQ2
GND  GND
DG10  A5
DG9  A4
DG8  A3
DG7  A2
DG6  A1
DG5  A0
DG4  GND
DG3  GND
DG2  GND
DG1  GND
DG0  GND
Vcc
Vcc - 59
60 - Vcc

SSRAM Expansion Pinout
(top view)

Vcc - 1  2 - Vcc
Vcc  Vcc
DQ14  DQ15
DQ13  DQ16
DQ12  DQ2
GND  GND
DG10  A5
DG9  A4
DG8  A3
DG7  A2
DG6  A1
DG5  A0
DG4  GND
DG3  GND
DG2  GND
DG1  GND
DG0  GND
Vcc
Vcc - 59
60 - Vcc
Setup and Usage

1. Make sure that all the ICs are properly mounted and that the FPGA is securely in its socket. The FPGA should be flush with the edges of the socket.

2. Install any option cards (RAM expansion and/or FPC).

3. Install the clock termination jumper if the RAM option card is not installed. Do not install the clock termination jumper if the RAM option card is installed since the RAM option card has a built-in clock terminator.

4. Install the master/slave select jumpers. Please refer to the diagram on the previous page for jumper installation orientation. Note that all the jumpers for each mode must be installed for the RHP4K to configure correctly. You should install a total of six jumpers.

5. Configure the node ID DIP switch if you are planning on using the scalable bus feature. If you are not planning on using the scalable bus feature, then the setting of the node ID DIP switch is ignored.

6. Install daisy-chain configuration cables if this device is part of a multiprocessor network.

7. Attach the RHP4K to the host computer via the IEEE1284 port using an IEEE1284 compliant cable.

8. Apply power to the board by plugging in the power connector.

9. The RHP4K is now ready for configuration via host software. Contact Xtreme Ideas Technology Development for sample code and programs for RHP4K configuration.